Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **NC**
2. **CAP+**
3. **GND**
4. **CAP-**
5. **VOUT**
6. **LV**
7. **OSC**
8. **V+**

**.078”**

**8**

**1**

**2 3**

**4**

**7 6 5**

**.077”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: V+**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .077” X .078” DATE: 8/25/21**

**MFG: HARRIS/INTERSIL THICKNESS .014” P/N: ICL7660**

**DG 10.1.2**

#### Rev B, 7/1